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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

18/Appeal Brief
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In re application of:

Yasutaka SAKAINO et al.

Serial No.: 09/229,628

Filed: January 13, 1999

For: SEMICONDUCTOR INTEGRATED CIRCUIT

Art Unit: 2814
Examiner: Mr. Phat X. Cao

Atty. Docket No. 32014-141666

Customer No.
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APPELLANT'S BRIEF ON APPEAL

Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

This Brief is being submitted under the provisions of 35 U.S.C. § 1.134 and 37 C.F.R. § 1.192 in support of an appeal from the final rejection of claims 3-5 and 16-21 of the subject application. A Notice of Appeal from the final rejection of claims 3-5 and 16-21 was timely filed on January 9, 2002. A copy of claims 3-5 and 16-21 are included in Appendix of this Brief. The Brief is being submitted in triplicate, together with the requisite fee of $310.00 as set forth in 37 C.F.R. § 1.17(c).

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1. REAL PARTY IN INTEREST

The real party in interest is OKI ELECTRIC INDUSTRY, CO., LTD.

2. RELATED APPEALS AND INTERFERENCES

To the best of the undersigned's belief, there are no related appeals or interference that will be directly affected by or have a bearing on the Board's decision in this appeal.

3. STATUS OF CLAIMS

The application as filed included claims 1-15. Claims 1-5 were rejected and claims 6-15 were allowed in the Office Action of September 13, 2000. Claims 1 and 2 were cancelled, claims 3-15 amended, and claims 16-21 added by an Amendment filed February 13, 2001. Claims 3-5 and 16-21 were finally rejected over the cited art by the Office Action mailed October 22, 2001. An Amendment After Final Rejection was filed November 29, 2001 amending claims 3, 5, and 20. The rejection of claims 16-21 under 35 U.S.C. §112, first paragraph in the Office Action of October 22, 2001 was withdrawn in the Advisory Action of December 19, 2001.

4. STATUS OF AMENDMENTS

An Amendment After-Final canceling claims 1 and 2 and amending claims 3, 5, and 20 was filed on November 29, 2001. An Advisory Action mailed December 19, 2001 indicates the Amendment After-Final will be entered for the purposes of Appeal. At this point, claims 6-15 are

allowed, and claims 3-5 and 16-21 are rejected.

5. SUMMARY OF THE INVENTION

The present invention relates to a semiconductor integrated circuit and to a layout pattern for such a circuit. The present invention provides a semiconductor layout which lowers the overall resistance value of conductors in the semiconductor integrated circuit compared to prior art layouts. The semiconductor layout of the present invention achieves a current that is only reduced 44% compared to that of a hypothetical ideal. In contrast to the present invention, a current flow in prior art layouts is reduced more than 64% compared to the ideal, page 6, line 20 - page 7, line 2 (all references to page and line numbers of the application refer to the Substitute Specification filed November 29, 2001).

These and other advantages are achievable utilizing a semiconductor device as recited, for example, in independent claim 3 and shown in Figures 1, 6A and 6B. According to an embodiment of the present invention shown in Figure 1, for example, a source 105 and a drain 106 are formed in a semiconductor substrate. A polysilicon layer 102 forming a first high resistance wiring layer and a first metal layer 103 forming a second low resistance wiring layer are formed over regions of the source 105 and drain 106, page 4, lines 18-20. As is shown in Figure 1, separate polysilicon layers 102 and first metal layers 103 can be provided for each of the source 105 and the drain 106, although the same reference numbers are used for the source 105 and the drain 106. The source 105 and drain 106 are connected to respective conductors, being the polysilicon layer 102 forming the

first high resistance wiring layer, via a plurality of first contacts 101. The first contacts 101 may be formed having a size, for example, of 0.6 microns by 0.7 microns. The contacts of this size result in a contact resistance between the source or drain and the first wiring layer 102 of 170 Ω/unit in terms of sheet resistance, page 4, lines 21 - page 5, line 2.

The conductors in the first high resistance wiring layer 102 over the source 105 and drain 106 are connected to the respective conductors in the second low resistance wiring layer 103 by a plurality of second contacts 104. The second contacts may be formed having a size of 0.7 microns by 0.7 microns. This results in a contact resistance between the first wiring layer 102 and the second wiring layer 103 being 9.5 Ω/unit in terms of sheet resistance, page 5, lines 3-8. The total number of first contacts 101 is greater than the total number of second contacts 104 as is recited in claim 3 and shown in Figure 1. In a preferred embodiment, the number of first contacts 101 is more than twice the number of second contacts 104 as recited in claim 16, see page 5, lines 12-16.

Utilizing a layer pattern having a greater number of first contacts than second contacts as recited in claims 3 and 16, the overall ON resistance of a transistor formed using the embodiment described above is 68.8 Ω, whereas the overall ON resistance of a prior art layout is 88.4 Ω . An I-V characteristic for a transistor using a layout according to the present invention is shown in Figure 2. With a transistor using the layout of the present invention, a current flow that is only reduced 44% compared to ideal current flow can be achieved. In comparison, a current flow of a transistor using conventional prior art layouts is reduced by more than 64% compared to ideal current flow. Accordingly, by using the present invention, an improvement of 20% in current flow can be

achieved. This is due to the overall contact resistance being reduced, resulting in an improvement in current driving capability, page 6, line 4 - page 7, line 7.

Independent claim 16 is similar to independent claim 3 and recites the number of first and third contacts 101 being more than twice the number of second and fourth contacts 104, respectively.

6. ISSUES

There is one issue in this appeal: Has the Examiner established that claims 3-5 and 16-21 are unpatentable under 35 U.S.C. § 103(a) over the prior art, particularly JP 6-232345 to Ando and U.S. Patent No. 5,844,281 to Narita.

7. GROUPING OF CLAIMS

Claims 3-5 stand or fall together, and claims 16-21 stand or fall together.

8. ARGUMENT

Claims 3-5 and 16-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over JP 6-232345 to Ando in view of U.S. Patent No. 5,844,281 to Narita. The cited references do not render the present invention obvious, since, among other things, they do not teach or suggest the number of contacts in the first contact group being different or more than twice the number of contacts in the second contact group and the number of contacts in the third contact group being different or more than twice as large as the number of contacts in the fourth contact group as is

recited in claims 3 and 16.

For example, referring to Figure 1, an embodiment of a semiconductor circuit device as recited in claim 3 comprises a source region 105 formed on a semiconductor substrate. A first conductor 102 having a first resistivity is formed over the source region 105, page 4, lines 18-20. A first contact group 101 having contacts is provided to connect the source region 105 and the first conductor 102, page 4, lines 21-23. A second conductor 103 having a second resistivity is provided over the first conductor 102, page 4, lines 18-23. A second contact group 104 having contacts is provided for connecting the first conductor 102 and the second conductor 103, page 5, lines 3-8. A drain region 106 is also formed on the semiconductor substrate. A third conductor 102 having the first resistivity is formed over the drain region 106, page 4, lines 18-20. A third contact group 101 having contacts is provided to connect the drain region 106 and the third conductor 102, page 4, lines 21-23. A fourth conductor 103 having the second resistivity is formed over the third conductor 102. A fourth contact group 104 having contacts is provided for connecting the third conductor 102 and the fourth conductor 103, page 5, lines 3-7. A total number of contacts in the first contact group 101 is different from a total number of contacts in the second contact group 104, and a total number of contacts in the third contact group 101 is different from a total number of contacts in the fourth contact group 104, page 5, lines 9-16 and Figures 1, 6A and 6B.

In comparison, Ando does not disclose having a different number of first contacts and second contacts, let alone twice as many second contacts. As shown in Figure 1A accompanying the Abstract of Ando, contact hole 106 connects the high resistance wiring layer 104 with the

source/drain part 103 of the transistor. Contact hole 105 connects the high resistance wiring layer 104 to a low resistance wiring layer, such as wiring layer 102. It is clearly shown in Figure 1A that the number of contacts 106 are the **same** as the number of contacts 105. Thus, Ando does not disclose the number of first contacts being **different** or **twice the number** of second contacts as recited in the rejected claims.

Narita does not supplement Ando to teach or suggest the total number of first contacts being different from the total number of second contacts as recited in claim 3 or that the total number of first contacts 101 is different from the total number of second contacts 102 as recited in independent claim 3 or the total number of first and third contacts 101 being more than twice the number of second contacts and fourth 104 as recited in independent claim 16.

Narita describes a semiconductor integrated circuit having an electrostatic protective function. Transistor 101 shown in Figures 1 and 2 of Narita includes a source diffusion layer 51. A grounding wire, corresponding arguably to the low resistance wire 103 of the present invention, is formed from an aluminum wire and connected to a tungsten silicide wire 11, corresponding arguably to the high resistance wiring layer 102 of the present invention, via a first contact 71. The tungsten silicide wire 11 is connected to the source diffusion layer 51 via a second contact 72, column 5, lines 21-41 of Narita. As is shown in Figures 1 and 2 of Narita, the first contact 71 and second contact 72 are arranged in **an alternating fashion**. Only a single wire layer is formed over the drain of the transistor 101 as shown in Figure 1 of Narita. Consequently, **only one type of contact**, namely the first contact 71, is formed over the drain.

Thus, both Ando and Narita disclose an alternating contact arrangement over the source. Therefore, combining the alternating contact scheme shown in Figure 1 of Narita with the structure of Ando results in **no change** to the alternating contact scheme shown in Ando. Both Ando and Narita disclose an arrangement of first and second contacts in alternating fashion. Ando shows contacts 105, 106 arranged in alternating order over the source region 103 and Narita shows contact 71 and 72 arranged in an alternating order over the source 51. Ando teaches the same number of contacts for a two wiring layer device, and Narita teaches an additional contact for a single wiring layer device. A combination of these references does not result in a semiconductor device having the number of first contacts being different from a number of second contacts in the second contact group and a number of third contacts being different from a number of fourth contacts as recited in claim 3 or the number of first contacts being more than twice as large as the number of second contacts and the third number of contacts being more than twice as large as the fourth number of contacts as recited in independent claim 16.

The Advisory Action of December 19, 2001 asserts Ando discloses two level wiring over the source and drain regions and Narita discloses the number of contacts in a first wiring group being different from a number of holes in a second wiring group. Figure 1 of Narita does disclose that a number of first contacts is greater than the number of second contacts. However, this is due to the use of **only a single wiring layer over the drain region** of transistor 101. In comparison, the claims of the present invention require two wiring layers over both the source and the drain. If the two-level wiring of the device of Ando were modified to include a different number of contacts using the

single wiring layer over the drain region of Narita, such a combination would not include two wiring layers over both the source region and the drain region as required by independent claims 3 and 16. Alternatively, if the two-level wiring of the device of Ando were modified to incorporate the alternating arrangement of first contact 71 and second contact 72 shown in the two layer wiring arrangement over the source region of Narita, such combination, as described above, would result in no change to the device of Ando.

Consequently, it is clear that the cited references, taken alone or in any combination, do not teach or suggest the features of the present invention.

9. CONCLUSION

It is respectfully submitted claims 3-5 and 16-21 are patentable over Ando and Narita and it is requested that the rejection of these claims be reversed. Thus, such combination does not result in combination of these references does not result in a semiconductor device having the number of first contacts being different from a number of second contacts in the second contact group and a number of third contacts being different from a number of fourth contacts as recited in claim 3 or the number of first contacts being more than twice as large as the number of second contacts and the third number of contacts being more than twice as large as the fourth number of contacts as recited in independent claim 16.

Respectfully submitted,

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10. APPENDIX

3. A semiconductor integrated circuit device, comprising:

a source region formed on a semiconductor substrate;

a first conductor having a first resistivity formed over said source region;

a first contact group having contacts connecting said source region and said first conductor;

a second conductor having a second resistivity over said first conductor;

a second contact group having contacts connecting said first conductor and said second conductor;

a drain region formed on said semiconductor substrate;

a third conductor having said first resistivity formed over said drain region;

a third contact group having contacts connecting said drain region and said third conductor;

a fourth conductor having said second resistivity formed over said third conductor;

a fourth contact group having contacts connecting said third conductor and said fourth conductor;

wherein a total number of contacts in said first contact group is different from a total number of contacts in said second contact group, and

a total number of contacts in said third contact group is different from a total number of contacts in said fourth contact group.

4. The semiconductor integrated circuit device as claimed in claim 3, wherein the total number of contacts in said first contact group is the same as the total number of contacts in said third contact group, and the total number of contacts in said second contact group is the same as the total number of contacts in said fourth contact group.

5. The semiconductor integrated circuit device as claimed in claim 4, wherein said first resistivity is higher than said second resistivity, and a total number of contacts in said first contact group and in said third contact group is greater than a total number of contacts in said second contact group and in said fourth contact group.

16. A transistor for use in an input protection circuit that protects circuitry fabricated on a semiconductor substrate, said transistor comprising:

a source region formed on the semiconductor substrate;

a first conductor having a first resistance formed over the source region;

a first number of first contacts connecting said source region and said first conductor;

a second conductor having a second resistance which is lower than the first resistance, said second conductor being formed over said first conductor;

a second number of second contacts connecting said first and second conductors;

a drain region formed on the semiconductor substrate;

a third conductor having the first resistance formed over the drain region;

a third number of third contacts connecting said drain region and said third conductor;

a fourth conductor having the second resistance formed over said third conductor;

a fourth number of fourth contacts connecting said third and fourth conductors;

a gate insulating layer formed on the semiconductor substrate between said source and drain regions; and

a gate electrode formed on the gate insulating layer,

wherein the first number is more than twice as large as the second number, and

wherein the third number is more than twice as large as the fourth number.

17. A transistor according to claim 16, wherein the first number is equal to the third number and the second number is equal to the fourth number.

18. A transistor according to claim 16, wherein said second contacts are located over end portions of said source region and said first contacts holes are located over a central portion of said source region.

19. A transistor according to claim 16, wherein said fourth contacts are located over end portions of said drain region and said third contacts are located over a central portion of said drain region.

20. A transistor according to claim 16, wherein a distance from an end of the source region to a nearest one of the first contacts is equal to or greater than a distance from the gate electrode to said nearest one of the first contacts.

21. A transistor according to claim 16, wherein a distance from an end of the drain region to a nearest one of the third contacts is equal to or greater than a distance from the gate electrode to said nearest one of the third contacts.